

**AMENDMENTS TO THE CLAIMS**

1-20. (Cancelled)

21. (Currently Amended) A nitride semiconductor LED, comprising:

a substrate;

a buffer layer on the substrate, wherein the buffer layer has a triple-structured  $Al_yIn_xGa_{1-(x+y)}N/In_xGa_{1-x}N/GaN$  laminated (where  $0 < x \leq 1$ ,  $0 \leq y \leq 1$ );

$Al_yGa_{1-y}N/GaN$  short period superlattice (SPS) layers on the buffer layer in a sandwich structure of upper and lower layers having an undoped GaN layer interposed therebetween (where  $0 < y \leq 1$ );

a first GaN based layer on the upper  $Al_yGa_{1-y}N/GaN$  SPS layer;

an active layer on the first GaN based layer; and

a second GaN based layer formed on the active layer.

22. (Cancelled)

23. (Previously Presented) The nitride semiconductor LED of claim 21, comprising an undoped GaN layer or an indium-doped GaN layer on the buffer layer, wherein the first GaN based layer is n type GaN based layer and the second GaN based layer is p type GaN based layer.

24. (Currently Amended) A nitride semiconductor LED, comprising:

a substrate;

a buffer layer on the substrate;

$\text{Al}_y\text{Ga}_{1-y}\text{N}/\text{GaN}$  short period superlattice (SPS) layers on the buffer layer in a sandwich structure of upper and lower layers having ~~an undoped GaN layer or an indium-doped GaN layer~~ interposed therebetween (where  $0 < y \leq 1$ );

a first GaN based layer above ~~and in direct contact with~~ the upper  $\text{Al}_y\text{Ga}_{1-y}\text{N}/\text{GaN}$  SPS layer;

an active layer above and in direct contact with the first GaN based layer; and

a second GaN based layer formed on the active layer.

25. (Previously Presented) The nitride semiconductor LED of claim 24, wherein the buffer layer has a triple-structured  $\text{Al}_y\text{In}_x\text{Ga}_{1-(x+y)}\text{N}/\text{In}_x\text{Ga}_{1-x}\text{N}/\text{GaN}$  laminated (where  $0 \leq x \leq 1$ ,  $0 \leq y \leq 1$ ), a double-structured  $\text{In}_x\text{Ga}_{1-x}\text{N}/\text{GaN}$  laminated (where  $0 \leq x \leq 1$ ), or a super-lattice-structured (SLS)  $\text{In}_x\text{Ga}_{1-x}\text{N}/\text{GaN}$  laminated (where  $0 \leq x \leq 1$ ) or a single crystalline layer.

26. (Previously Presented) The nitride semiconductor LED of claim 24, comprising an undoped GaN layer or an indium-doped GaN layer on the buffer layer, wherein the first GaN based layer is n type GaN based layer and the second GaN based layer is p type GaN based layer.

27. (Currently Amended) A nitride semiconductor LED, comprising:

a substrate;

a buffer layer on the substrate;

~~an undoped GaN layer or an indium-doped GaN layer on the buffer layer;~~

~~Al<sub>y</sub>Ga<sub>1-y</sub>N/GaN short period superlattice (SPS) layers on the undoped GaN layer or the indium-doped GaN layer, in a sandwich structure of upper and lower layers having the undoped indium-doped GaN layer interposed therebetween (where 0 < y ≤ 1);~~

a first n type GaN based layer on the upper Al<sub>y</sub>Ga<sub>1-y</sub>N/GaN SPS layer and containing a high concentration of dopants;

a second n type GaN based layer on the first n type GaN based layer;

an active layer on the second n type GaN based layer; and

a first p type GaN based layer on the active layer.

28. (Previously Presented) The nitride semiconductor LED of claim 27, wherein the buffer layer has a triple-structured Al<sub>y</sub>In<sub>x</sub>Ga<sub>1-(x+y)</sub>N/In<sub>x</sub>Ga<sub>1-x</sub>N/GaN laminated (where 0 ≤ x ≤ 1, 0 ≤ y ≤ 1), a double-structured In<sub>x</sub>Ga<sub>1-x</sub>N/GaN laminated (where 0 ≤ x ≤ 1), or a super-lattice-structured (SLS) In<sub>x</sub>Ga<sub>1-x</sub>N/GaN laminated (where 0 ≤ x ≤ 1) or a single crystalline layer.

29. (Previously Presented) The nitride semiconductor LED of claim 27, wherein the dopant concentration of the first n type GaN based layer is more than 1x10<sup>18</sup>/cm<sup>3</sup>.

30. (Previously Presented) The nitride semiconductor LED of claim 27, wherein the dopant concentration of the second n type GaN based layer is less than 1x10<sup>18</sup>/cm<sup>3</sup>.

31. (Currently Amended) A nitride semiconductor LED, comprising:

a substrate;

a buffer layer on the substrate, wherein the buffer layer has a triple-structured  $\text{Al}_y\text{In}_x\text{Ga}_{1-(x+y)}\text{N}/\text{In}_x\text{Ga}_{1-x}\text{N}/\text{GaN}$  laminated (where  $0 < x \leq 1$ ,  $0 \leq y \leq 1$ );

an undoped GaN layer or an indium-doped GaN layer on the buffer layer;

$\text{Al}_y\text{Ga}_{1-y}\text{N}/\text{GaN}$  short period superlattice (SPS) layers on the undoped GaN layer or the indium-doped GaN layer, in a sandwich structure of upper and lower layers having the undoped GaN layer or the indium-doped GaN layer interposed therebetween (where  $0 < y \leq 1$ );

a first n type GaN based layer above and in direct contact with the upper  $\text{Al}_y\text{Ga}_{1-y}\text{N}/\text{GaN}$  SPS layer and containing a high concentration of dopants;

a second n type GaN based layer on the first n type GaN based layer;

an active layer on the second n type GaN based layer; and

a first p type GaN based layer on the active layer.

32. (Cancelled)

33. (Previously Presented) The nitride semiconductor LED of claim 31, wherein the dopant concentration of the first n type GaN based layer is more than  $1 \times 10^{18}/\text{cm}^3$ .

34. (Previously Presented) The nitride semiconductor LED of claim 31, wherein the dopant concentration of the second n type GaN based layer is less than  $1 \times 10^{18}/\text{cm}^3$ .

35. (Currently Amended) A fabrication method of a nitride semiconductor LED, the method comprising the steps of:

forming a buffer layer on a substrate, wherein the buffer layer has a triple-structured  $\text{Al}_y\text{In}_x\text{Ga}_{1-(x+y)}\text{N}/\text{In}_x\text{Ga}_{1-x}\text{N}/\text{GaN}$  laminated (where  $0 < x \leq 1$ ,  $0 \leq y \leq 1$ );  
forming  $\text{Al}_y\text{Ga}_{1-y}\text{N}/\text{GaN}$  short period superlattice (SPS) layers on the buffer layer in a sandwich structure of upper and lower layers having an undoped GaN layer or an indium-doped GaN layer interposed therebetween (where  $0 < y \leq 1$ );  
forming a first GaN based layer above and in direct contact with the upper  $\text{Al}_y\text{Ga}_{1-y}\text{N}/\text{GaN}$  SPS layer;  
forming an active layer on the first GaN based layer; and  
forming a second GaN based layer formed on the active layer.

36. (Previously Presented) The fabrication method of claim 35, comprising a step of forming an n-GaN layer containing a low concentration of dopants, between the first GaN based layer of a  $\text{n}^+$ -GaN layer and the active layer.

37. (Cancelled)

38. (Previously Presented) The fabrication method of claim 35, comprising forming an undoped GaN layer or an indium-doped GaN layer on the buffer layer, wherein the first GaN based layer is n type GaN based layer and the second GaN based layer is p type GaN based layer.

39. (Previously Presented) The fabrication method of claim 35, wherein forming the buffer layer is, using a MOCVD equipment, grown-up to have a 50-800 Å thickness at a 500-800 °C temperature and in an atmosphere having H<sub>2</sub> and N<sub>2</sub> carrier gases supplied while having TMGa, TMIn, TMAI source gas introduced and simultaneously having NH<sub>3</sub> gas introduced.

40. (Previously Presented) The fabrication method of claim 35, wherein the dopant concentration of the first GaN based layer is more than 1x10<sup>18</sup>/cm<sup>3</sup>.